Analog Realization of a Low-Voltage Sixteen Selectable Fractional-Order Differentiator in a 0.35um CMOS Technology

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***Abstract*—This paper presents the design and implementation of an analog fractional-order differentiator (FOD) in a microelectronics scale. It focused on the design and implementation of sixteen selectable fractional-order (0.10, 0.20, 0.25, 0.30, 0.35, 0.40, 0.45, 0.50, 0.55, 0.60, 0.65, 0.70, 0.75, 0.80, 0.85 and 0.90) differentiators in a 0.35um CMOS technology operated at 1.5-V supply. In comparison with the previous work that uses generic microcontroller for switching an FOD from one order to the next, this design of a 16 selectable FOD was realized in an analog microelectronic scale, thus, the physical implementation is relatively smaller. The authors employed reusability of resistors and capacitors when switching from one order to the other. The RC ladder in the design was implanted using NMOS capacitor and NWELL resistors while the IC design was implemented using TANNER software. The whole chip layout of the design has a dimension of 11.55mm x 8.32mm or equivalent to a final area of 96.10mm2. Each fractional order was characterized in terms of its frequency response —magnitude and phase response—in the bandwidth from 10Hz to 1kHz.**

***Index Terms*—constant phase element, resistor-capacitor ladder, selectable fractional-order differentiator, CMOS**

I. Introduction

THE concept of fractional calculus dates back to the time of Leibniz and L'Hospital in 1695 [1]. It is based on calculus with derivatives and integrals having non-integer orders. The concept fractional order calculus has not been easily adapted due to the complexity of its realization. Some definitions have been used for the general fractional calculus such as the Grunwald-Letnikov (GL) and the Riemann-Liouville (RL) [2]. Recently, it became a powerful and widely used tool for dynamical systems modeling [3], [4], [5], processes control [6], [7], [8], signal processing [9], [10], [11], and in many other fields of science and engineering.

Fractional-order differentiator (FOD) is a differentiator that performs non-integer-order differentiation, e.g. ½-order differentiation which is half derivative of a function. FOD can be realized through one of the following ways: a) Poly-Methyl-Methacrylate (PMMA) [12]; b) $LiN_2H_5SO_4$ or commonly known as the Lithium Salt [13]; c) Field Programmable Gate Arrays (FPGA) [14]; or d) electric component in the form of a Resistor-Capacitor (RC) ladder network [15], [16].

This paper focuses on the analog realization of a fractional-order differentiator implemented on a single integrated circuit (IC) design layout similar to the one presented in [17], [18].

II. Theory of Fractional-order Differentiator

A. Fractional Order Differentiator

A fractional-order differentiator is the generalization of a basic differentiator. An FOD can also be realized using operational amplifier (op-amp) circuit as shown in Figure 1. Instead of using a simple capacitor at its input side, an FOD uses a constant phase element (CPE).

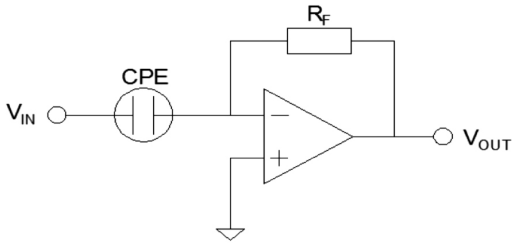

Fig. 1. Fractional-order differentiator circuit implementation

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According to [15], a fractional-order differentiator has a continuous-time transfer function of

$$G(s) = s^{\alpha} \quad (1)$$

wherein the magnitude of impedance depends on frequency according to the order of differentiation (α). Its value in decibels varies with the expression (20*α) dB/dec. Furthermore, the phase of the impedance is constant at the expression (90*α)°.

B. Constant Phase Element

An ideal constant phase element is composed of infinite number of lumped-sum parallel resistor-capacitor (RC) networks according to the concept of continued fraction expansions (CFE) representing an ideal transmission line [19]. Practically, the CPE in Figure 1 can be electronically realized using an RC ladder that approximates a fractional-order element with the schematic shown in Figure 2. This RC ladder was presented in [15] and was used successfully in the practical realization of fractional-order system.

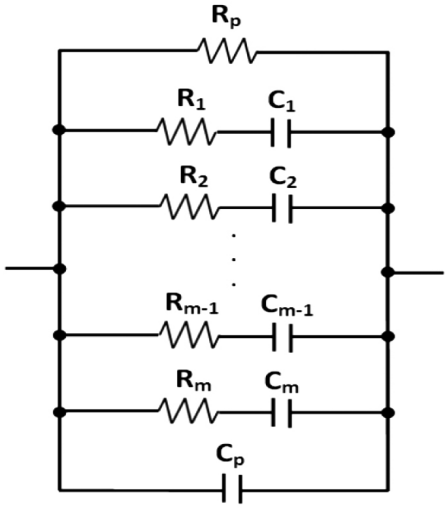

Fig. 2. CPE realization using RC ladder based on [15]

The following discussions of CPE was lifted from [15] and [18]. Generally, the higher the number of branches, the better the approximation of a CPE [15]. But for practical purposes, [15] and [18] only used five (5) branches in their CPE realization using RC-ladder network which is fit enough to meet the desired frequency band of interest. The method of RC ladder computation in this study are based primarily on [18] which is an improved and more general way compared to RC ladder network design presented in [16]. Table 1, which is based from [18], shows a summary comparing the original method of computation [16] and the optimized RC ladder branch values computation developed by the authors of this paper. The established optimization procedures developed by the authors are more general, straightforward and flexible since the recalibration step from the old method is eliminated. In effect, infinite sets of RC ladder can be obtained using the new approach which allows common values of resistor and capacitor for different fractional orders.

In the new CPE design procedure, four initial values are needed: 1) the maximum allowable phase ripple (Δφ); 2) the number of RC ladder branches (m); 3) the order of differentiation (α); and 4) the initial value of R_1 (same for all orders). The remaining nine values of resistors (R2 to R5) and capacitors (C1 to C5) for the ladder branch can be computed using equations (2) to (7) as follows:

TABLE I
COMPARISON OF THE ORIGINAL AND OPTIMIZED RC LADDER BRANCH VALUES COMPUTATION

STEPS	ORIGINAL COMPUTATION [15]	OPTIMIZED COMPUTATION
Initial values needed	Phase Ripple (Δϕ) Desired Gain (Dr) Order (α) No. of branch (m) Initial R1 and C1	Phase Ripple (Δϕ) Order (α) No. of branch (m) Initial R1
Determination of parameters 'a' and 'b'	$ab \approx \frac{0.24}{1+\Delta\varphi}$ $\log a = \alpha \log(ab)$	$ab = \frac{0.24}{1+\Delta\varphi}$ $\log a = \alpha \log(ab)$
Determination of RC ladder branch values	$R_k = R_1 a^{k-1}$ $C_k = C_1 b^{k-1}$	$R_k = R_1 a^{k-1}$ $C_k = \frac{b^{k-1}}{100R_1}$
Determination of 'Rp' and 'Cp'	$R_p = R_1 \frac{1-a}{a}$ $C_p = C_1 \frac{b^m}{1-b}$	$R_p = R_1 \frac{1-a}{a}$ $C_p = C_1 \frac{b^m}{100R_1(1-b)}$
Approximation of the minimum and maximum frequencies of operation	$\omega_{max} \approx \frac{\omega_{min}}{(ab)^m}$ $\omega_{av} = \sqrt{\omega_{max}\omega_{min}}$	$\omega_{max} \approx \frac{\omega_{min}}{(ab)^m}$ $\omega_{av} = \sqrt{\omega_{max}\omega_{min}}$
Recalibration of the resistor and capacitor values	$Y(j\omega) = \frac{1}{R_p} + j\omega C_p \ldots$ $\ldots + \sum_{k=1}^{m} \frac{j\omega C_k}{1 + j\omega R_k C_k}$ $D = \frac{1}{\lvert Y(j\omega_{av})\rvert \omega_{av}^{\alpha}}$ **Resistors multiplied by Dr/D** **Capacitors divided by Dr/D**	NO RECALIBRATION NEEDED

$$R_k = R_1 a^{k-1} \quad (2)$$

and

$$C_k = \frac{b^{k-1}}{100 R_1} \quad (3)$$

According to [15], the parameters 'a' and 'b' ranges between 0 and 1 which can be computed using their relationships with the order of differentiation (α) and the maximum allowable phase ripple (Δφ) as

$$\Delta\varphi = \frac{0.24}{ab} - 1 \tag{4}$$

and

$$\alpha = \frac{\log a}{\log (ab)} \tag{5}$$

To replace the truncated sections by a simple network for the CPE, the resistive side of the ladder (upper portion) can be represented by a single resistor R_p while the capacitive (lower portion) can be represented by a single capacitor C_p with values computed using

$$R_p = R_1 \frac{1-a}{a} \tag{6}$$

and

$$C_p = \frac{b^m}{100\, R_1 (1-b)} \tag{7}$$

For this study, the authors used phase ripple Δφ = 0.2, m = 5, R_1 = 200kΩ. The values for the sixteen fractional orders are α = ***0.10, 0.20, 0.25, 0.30, 0.35, 0.40, 0.45, 0.50, 0.55, 0.60, 0.65, 0.70, 0.75, 0.80, 0.85,*** and ***0.90.*** Table 2 shows the list of all the computed resistor and capacitor values for the sixteen fractional orders.

TABLE II
LIST OF ALL RESISTOR AND CAPACITOR VALUES FOR 16FOD RC LADDER NETWORK

ORDER	0.10	0.20	0.25	0.30	0.35	0.40	0.45	0.50
R1(Ω)	200000.00	200000.00	200000.00	200000.00	200000.00	200000.00	200000.00	200000.00
R2(Ω)	170267.98	144955.93	133748.06	123406.77	113865.06	105061.11	96937.87	89442.72
R3(Ω)	144955.93	105061.11	89442.72	76146.16	64826.26	55189.19	46984.76	40000.00
R4(Ω)	123406.77	76146.16	59813.95	46984.76	36907.23	28991.19	22773.01	17888.54
R5(Ω)	105061.11	55189.19	40000.00	28991.19	21012.22	15229.23	11037.84	8000.00
Rp(Ω)	34923.79	75945.93	99069.76	124131.32	151293.00	180730.79	212635.41	247213.60
ORDER	0.55	0.60	0.65	0.70	0.75	0.80	0.85	0.90
R1(Ω)	200000.00	200000.00	200000.00	200000.00	200000.00	200000.00	200000.00	200000.00
R2(Ω)	82527.08	76146.16	70258.60	64826.26	59813.95	55189.19	50922.00	46984.76
R3(Ω)	34053.60	28991.19	24681.35	21012.22	17888.54	15229.23	12965.25	11037.84
R4(Ω)	14051.72	11037.84	8670.39	6810.72	5349.92	4202.44	3301.08	2593.05
R5(Ω)	5798.24	4202.44	3045.85	2207.57	1600.00	1159.65	840.49	609.17
Rp(Ω)	284689.37	325305.56	369325.32	417033.86	468740.30	524779.66	585515.03	651339.92
ORDER	0.10	0.20	0.25	0.30	0.35	0.40	0.45	0.50
C1(F)	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08
C2(F)	1.1746E-08	1.3797E-08	1.4953E-08	1.6207E-08	1.7565E-08	1.9037E-08	2.0632E-08	2.2361E-08
C3(F)	2.7595E-09	3.8073E-09	4.4721E-09	5.2531E-09	6.1703E-09	7.2478E-09	8.5134E-09	1.0000E-08
C4(F)	6.4826E-10	1.0506E-09	1.3375E-09	1.7027E-09	2.1676E-09	2.7595E-09	3.5129E-09	4.4721E-09
C5(F)	1.5229E-10	2.8991E-10	4.0000E-10	5.5189E-10	7.6146E-10	1.0506E-09	1.4496E-09	2.0000E-09
Cp(F)	4.6763E-11	1.1049E-10	1.7067E-10	2.6467E-10	4.1235E-10	6.4592E-10	1.0183E-09	1.6180E-09
ORDER	0.55	0.60	0.65	0.70	0.75	0.80	0.85	0.90
C1(F)	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08	5.0000E-08
C2(F)	2.4234E-08	2.6265E-08	2.8466E-08	3.0852E-08	3.3437E-08	3.6239E-08	3.9276E-08	4.2567E-08
C3(F)	1.1746E-08	1.3797E-08	1.6207E-08	1.9037E-08	2.2361E-08	2.6265E-08	3.0852E-08	3.6239E-08
C4(F)	5.6933E-09	7.2478E-09	9.2268E-09	1.1746E-08	1.4953E-08	1.9037E-08	2.4234E-08	3.0852E-08
C5(F)	2.7595E-09	3.8073E-09	5.2531E-09	7.2478E-09	1.0000E-08	1.3797E-08	1.9037E-08	2.6265E-08
Cp(F)	2.5955E-09	4.2132E-09	6.9442E-09	1.1678E-08	2.0188E-08	3.6335E-08	6.9718E-08	1.5041E-07

III. CONCEPTUAL DESIGN OF A SELECTABLE FOD

A conceptual selectable fractional-order differentiator was shown in [16] using discrete components. The conceptual design's order of differentiation can be chosen from 0 to 1 with an increment of 0.05.

The design utilizes cascaded operational amplifiers and resistor-capacitor ladders as its main components, while a generic microcontroller is introduced for switching purposes. Initial simulation results through Matlab and LTSpiceIV show that the designed resistor-capacitor ladders can perform as an analog FOD [16].

For the sole purpose of switching circuitry, utilization of microcontroller apparently results to much lower component density in the hardware implementation. While the trend in electronics physical realization is to go smaller and lightweight, the authors were inspired to design and implement a sixteen selectable FOD in microelectronic scale using 0.35um CMOS technology. The whole design was implemented in a relatively much simpler architecture wherein the switching circuitry is already an integrated part of the whole circuit eliminating the use of microcontroller.

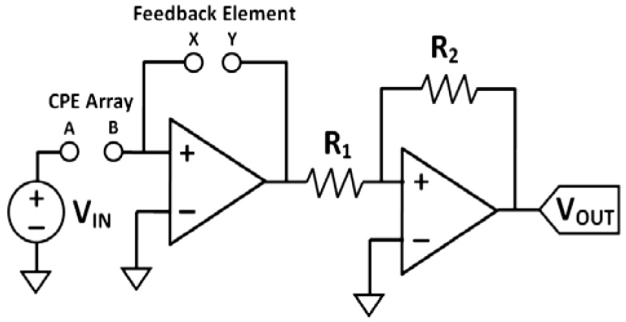

Fig. 3. Schematic layout of a selectable FOD utilizing selector module circuitry

Figure 3 shows the basic schematic overview of a selectable FOD. Basically, change of α would require a change of ladder values (see Table 2) as well as the value of feedback resistor (see Table 3). There will be two sets of selector module circuit: one for CPE module (pins A and B) and the other for feedback (pins X and Y). Table 3 also shows the magnitude gain of the FOD at different frequencies.

Reuse of resistors and capacitors was adopted in the design to further scale down the physical dimension of the implementation. This simply means that some of the RC components in one fractional order to another are being utilized as switching occurs. As can be observed in Table 2, all fractional orders have 200-kΩ R_1 and 50-nF C_1. Instead of having sixteen 200-kΩ R_1 and sixteen 50-nF C_1 in the circuit design, it is possible to have just one 200-kΩ R_1 and one 50-nF C_1 for all FODs. The concept of reusability was initially employed by the authors in two-order FOD (2FOD) design [18]. Generally, 16FOD is just an expansion of 2FOD.

TABLE III
MAGNITUDE GAIN AND CORRESPONDING R_F FOR 16FOD

ORDER	Magnitude Gain of the FOD (in dB)			Feedback Resistor (R_F) in Ω
	10Hz	100Hz	1kHz	
0.10	3.60	5.60	7.60	17k
0.20	7.19	11.19	15.19	51k
0.25	8.99	13.99	18.99	77k
0.30	10.79	16.79	22.79	110k
0.35	12.59	19.59	26.59	155k
0.40	14.39	22.39	30.39	206k
0.45	16.18	25.18	34.18	271k
0.50	17.98	27.98	37.98	351k
0.55	19.78	30.78	41.78	436k
0.60	21.58	33.58	45.58	531k
0.65	23.38	36.38	49.38	646k
0.70	25.17	39.17	53.17	716k
0.75	26.97	41.97	56.97	766k
0.80	28.77	44.77	60.77	804k
0.85	30.57	47.57	64.57	814k
0.90	32.37	50.37	68.37	816k

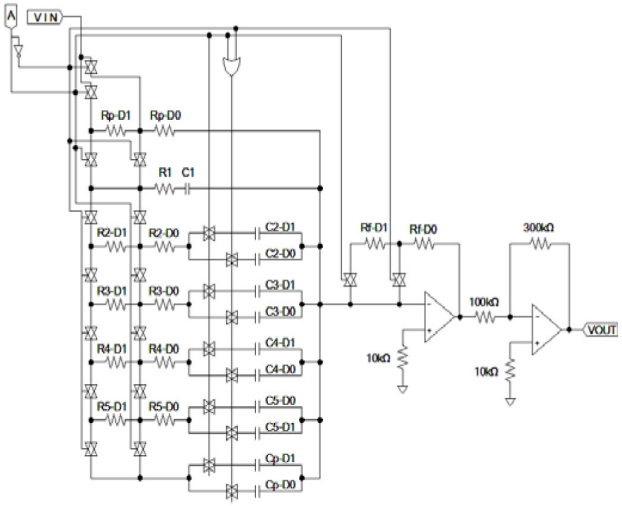

Fig. 4. Top-level schematic of a 2FOD [18]

An understanding of reusability can be simply deduced from Figure 4 which shows the top-level schematic of a two-order selectable FOD. The control bit A determines which order of differentiation to actuate: A="0" for FOD(0.25) and A="1" for FOD(0.50). The design utilizes

several transmission gates to switch from one order to the next. An OR gate is used for actuating set of capacitors. For both orders of differentiation, all capacitor D0's have to be activated. Capacitors D1's connected in parallel to capacitor D0's supplement the necessary capacitance values. The switch-activated RC ladder circuit serves as the input impedance to the two-stage CMOS operational amplifier that is then post-cascaded to another inverting amplifier [18].

Ideally, the magnitude of an FOD is 0dB at ω=1 rad/s. According to [16], the average frequency ω_{av} can be computed using the equation shown in Table 2. For instance, if the order of differentiation is 0.25, then the average frequency is around 5590.2 rad/s or equivalent to 890Hz. Using the closest decade point, which is at 1kHz, the magnitude of the gain should be at $|G(j\omega)|_{\omega=2\pi(1000)} = \omega^{0.25}|_{\omega=2\pi(1000)} = 8.9032$ which is around 18.99dB. Table 3 summarizes the magnitude gain for every decade from 10Hz to 1kHz, as well as the corresponding feedback resistor values empirically chosen for sixteen fractional orders of differentiation.

According to [18], the concept of reusability can be applied for other RC ladder branches. The magnitude of R_2 for FOD(0.50) from Table 2 can be reused and add up with 44305.34Ω to complete the 133748.06-Ω R_2 needed for FOD(0.25). Likewise, with the capacitor, the magnitude of C_2 for FOD(0.25) can be reused and add up with 7.4072nF to accummulate a total of 22.361-nF C_2 needed for FOD(0.50). This scheme significantly reduces the overall dimension of the analog realization since duplication of resistor and capacitor values is averted. Strategic placing of the transmission gates must be thoroughly taken into consideration to optimize reusability.

Figure 5 shows the top-level schematic of 16FOD which consists of a 4-bit parallel-in parallel-out (PIPO) register, a 4x16 line decoder, arrays of CPE elements, arrays of feedback resistor and cascaded inverting amplifiers. The design of 16FOD is very similar to anexpanded Figure 4. Resistor array and capacitor array magnification of CPE elements are shown in Figures 6 and 7 respectively after employing reusability for the sixteen fractional orders.

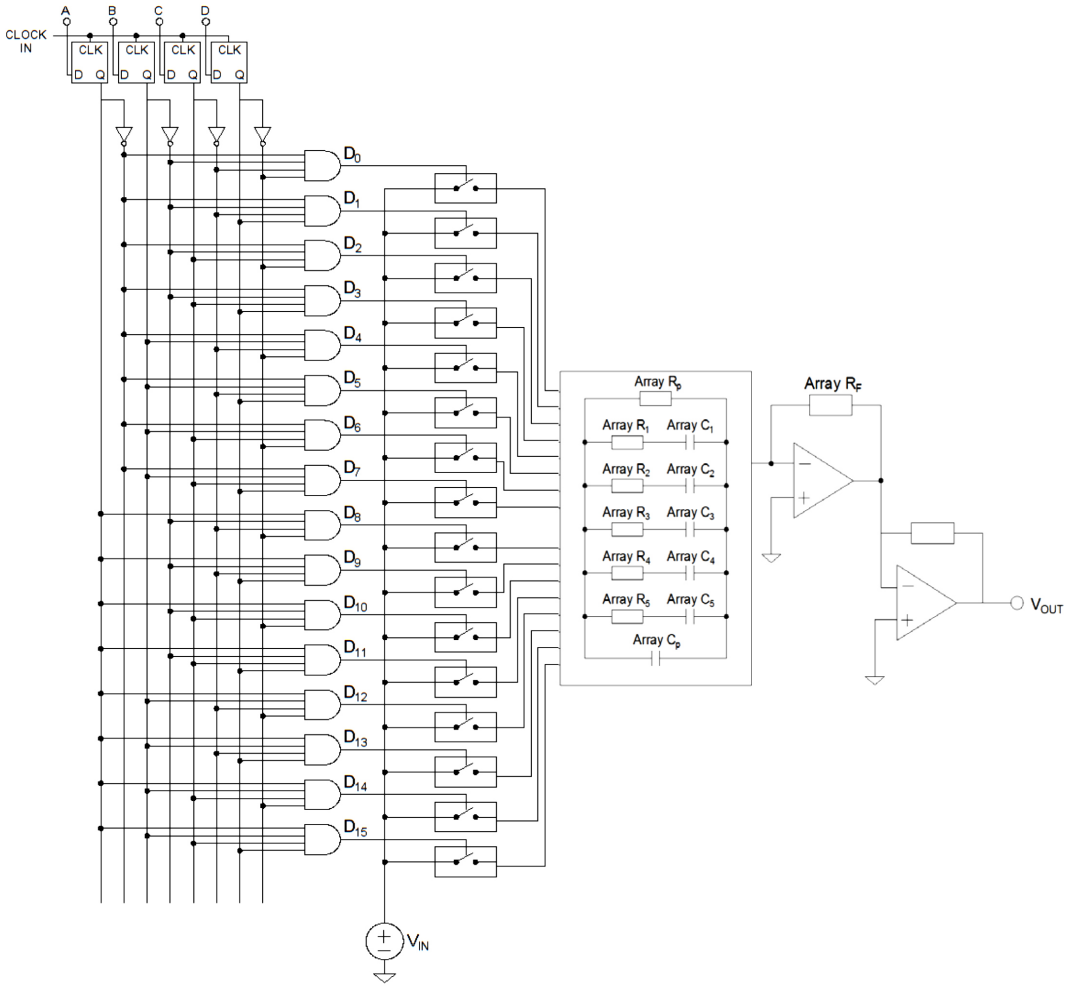

Fig. 5. Top-level schematic of a sixteen selectable FOD

The 4-bit PIPO register catches the input order of differentiation. If for instance all bits (A, B, C, D) are "low," FOD(0.10) is activated and if all bits are "high," FOD(0.90) is activated. Transmission gates in the RC arrays are all normally open. The 4x16 line decoder that signals which set of transmission gates to trigger, in essence, dictate which series-connected resistors and parallel-connected capacitors to add up. This scheme also applies for the array of feedback resistors. The output of each resistor array branch is cascaded to its corresponding capacitor array to generate the necessary input impedance for the inverting operational amplifier.

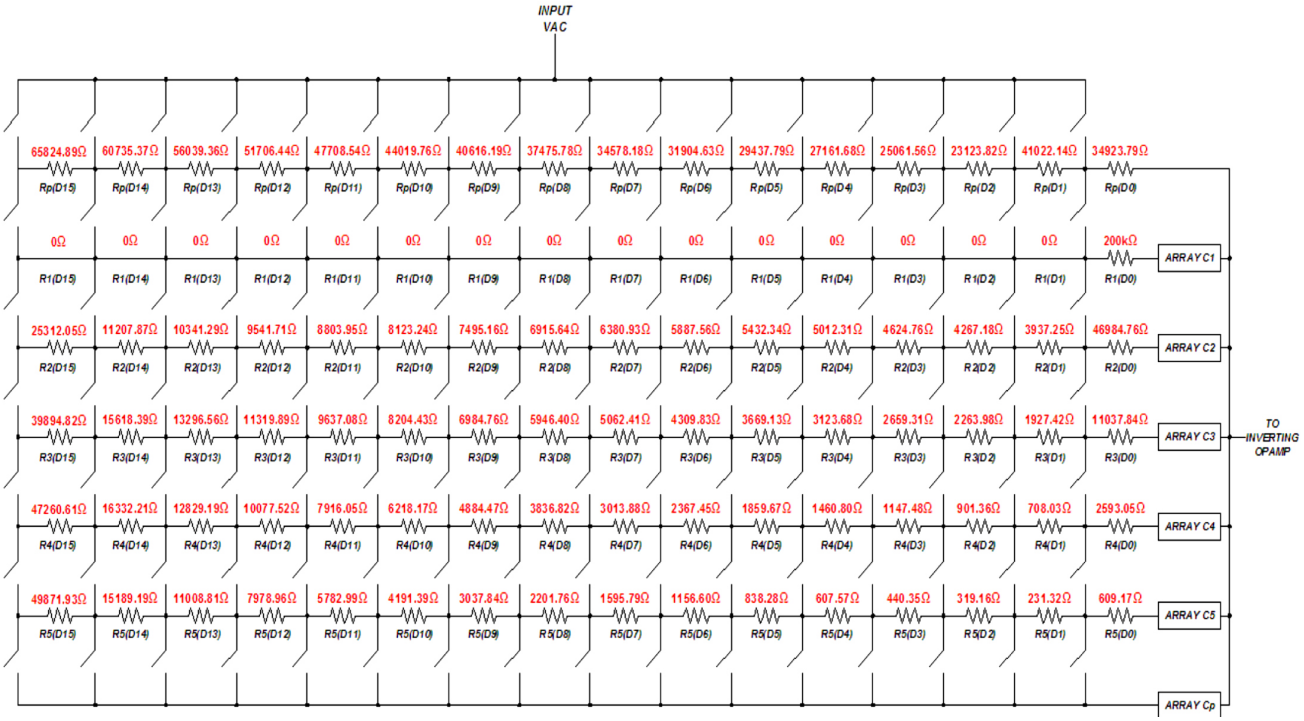

Fig. 6. Resistor array of CPE employing reusability for selectable 16FOD

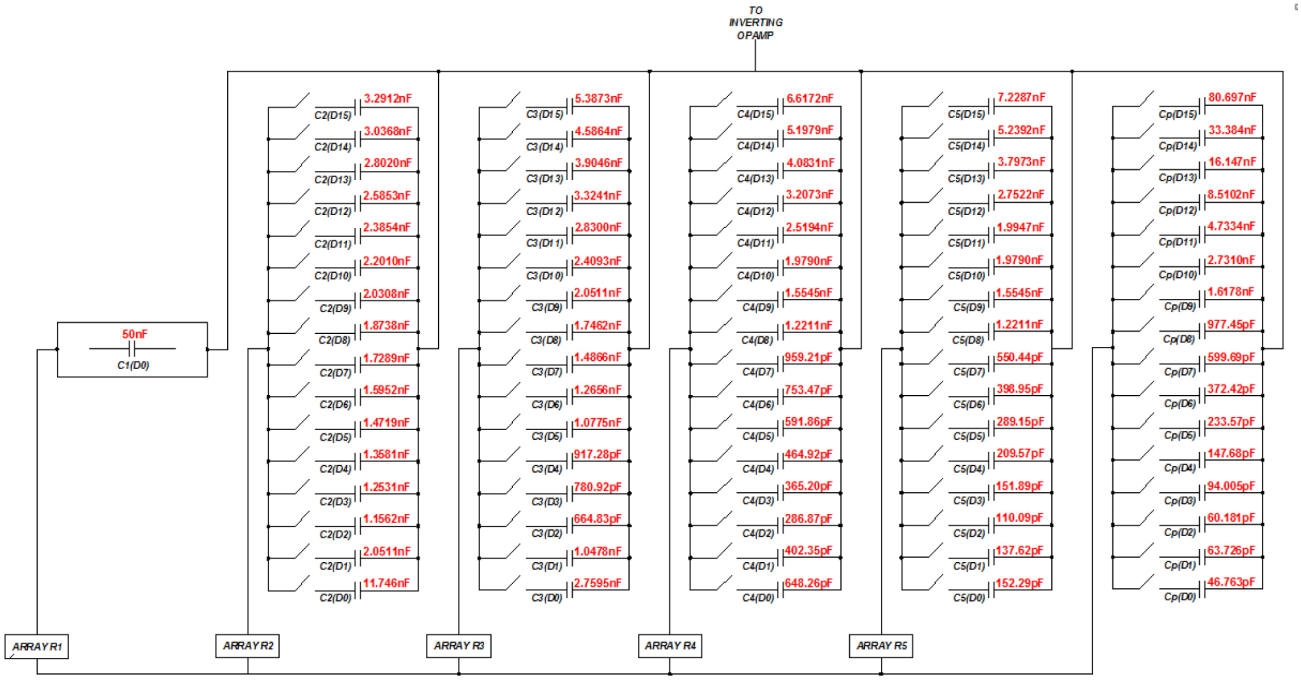

Fig. 7. Capacitor array of CPE employing reusability for selectable 16FOD

IV. Integrated Circuit (IC) Layout Implementation

Like the layout designs in [17] and [18], Tanner Software was also used to produce a single-chip layout of the whole circuit in this study. L-edit tanner tool was used as the layout editor.

A. Operational Amplifier CMOS Module

The op-amp used in [18], [20], [21] shown in Figure 5 was adopted for this study. The design works at low voltage supply of around 1.5 volts instead of the typical 3.3V for 0.35um CMOS technology. The adopted op-amp can be operated either by using unipolar or bipolar supply. It was designed to operate at +/-0.75V or 1.5V to GND. Either way, the op-amp exhibits same parametric response.

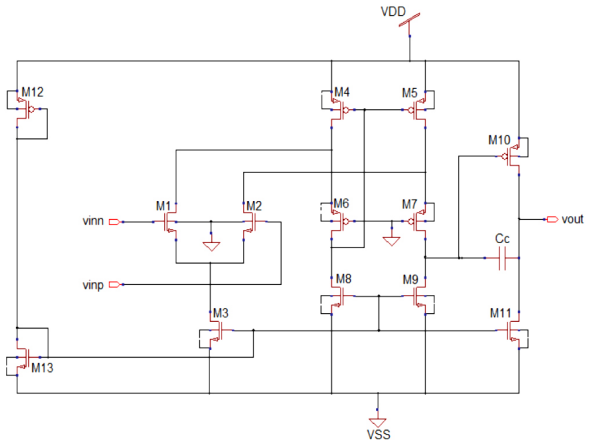

Fig. 8. Op-amp low voltage design [40]

Ideally, the voltage gain phase of the op-amp at 0dB should be at 45° and at least a gain of 60dB should be achieved. It is likewise important to ensure that all transistors are operating in saturation region. Step by step computation for the transistor sizes were guided by [20], [21], [22]. Table 4 shows the summary of the computed width size of transistors M1 to M11 alongside with its adjusted width size (actual size). A bias voltage of 0.65V is needed to operate the op-amp with its desired functionality. This can be achieved through the use of bias transistors M12 and M13 having values equal to 6um and 1um, respectively. All transistors have the length of 1um.

B. Experimental Validation Setup

The actual layout underwent physical verification processes through Design Rule Check (DRC), ensuring that the created mask layout conform to the complex set of design rules and Layout Verification Schematic (LVS) assuring it represents the circuit desired to be fabricated.

TABLE IV
Op-Amp Transistor Sizes Used for the Selectable FOD

Transistor	Computed Width Size (um)	Actual Width Size (um)
M1	12.15	17
M2	12.15	17
M3	24.30	16
M4	22.73	22
M5	22.73	22
M6	22.73	18
M7	22.73	18
M8	11.54	20
M9	11.54	20
M10	27.27	28
M11	11.5385	37

Parasitic capacitances were considered in the design to create an accurate analog model of the circuit. However, only nodal parasitic capacitance effects were counted in the simulation as this was the only option possible in the simulation software. Parasitic resistances and inductances were not included in the extraction. All nodal parasitic capacitances were considered since all capacitance less than 0 femtofarad were set to be ignored.

The ideal magnitude and phase response of an FOD for different orders are listed in Table 5, which was used to validate the frequency response. In reference to [16] and [18], ideal responses, specifically the phase response, are not attainable for the whole frequency band due to the gain-bandwidth limitation of the op-amp.

C. CMOS Layout View of a Selectable FOD

Shown in Figure 9 is the physical layout implementation of the 16FOD. It has an overall IC dimension of 11.55mm x 8.32mm. The total area of 16FOD is equivalent to just three times the layout of semi-differentiator presented in [17].

As shown in Figure 10, the microelectronic-scaled selectable FOD exhibits magnitude response that is almost equal to the ideal gain. On the other hand, the phase response significantly deviates from the ideal as the frequency increases. Table 5 presents the post-layout results of gain and phase response for the sixteen fractional orders. Not all FODs are working for this whole frequency band of interest. Theoretically, the RC ladder can perform the desired constant phase element. However, when incorporated in an op-amp circuit, the range of frequencies diminishes. This is mainly due to the characteristics and gain-bandwidth-product (GBP) limitation of the op-amp. For higher bandwidth applications, a design of op-amp with higher GBP is necessary.

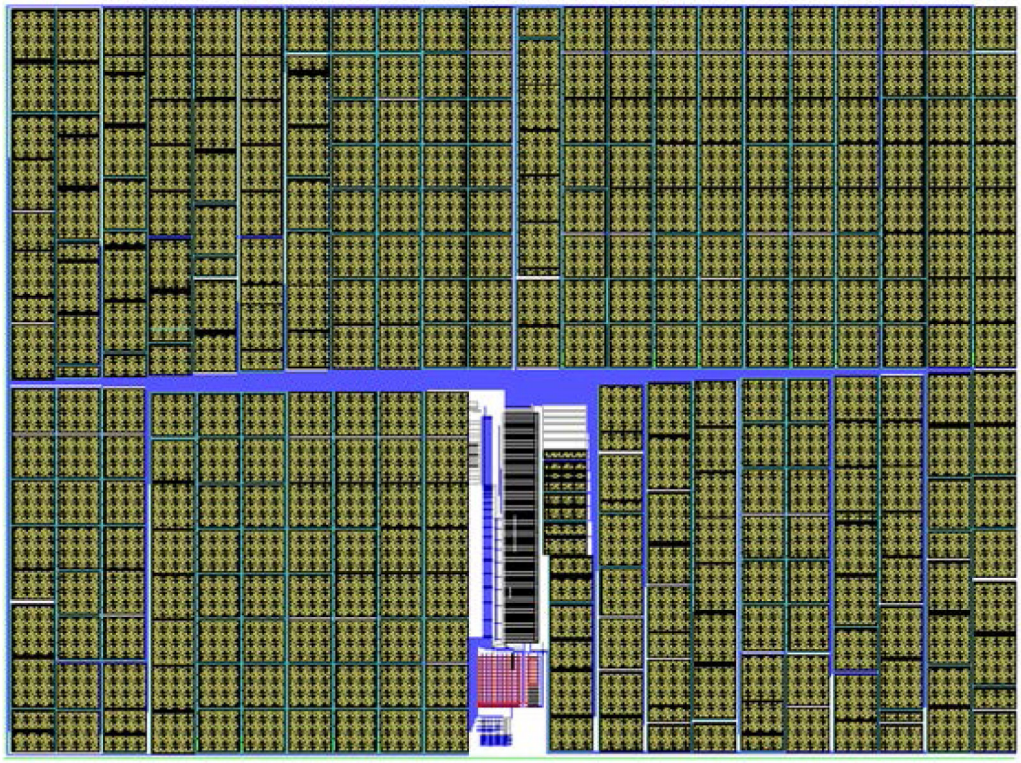

Fig. 9. Top-level layout of a selectable 16FOD

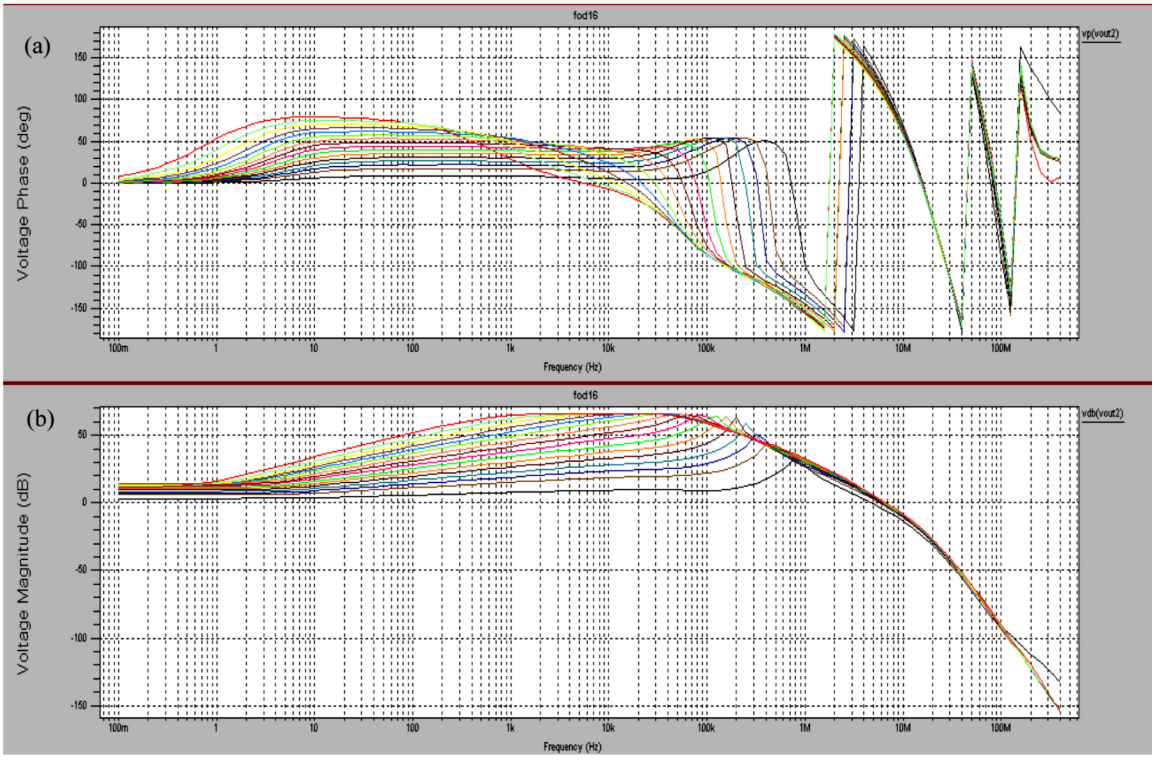

Fig. 10. Frequency response of the designed 16FOD for: a) phase response and b) magnitude response

TABLE V

6FOD GAIN AND PHASE RESPONSE

ORDER	FREQ	IDEAL GAIN (dB)	Post-Layout Results (dB)	IDEAL PHASE (degrees)	Post-layout Result (degrees)
FOD(0.10)	10Hz	3.60	3.83	9.0	6.02
	100Hz	5.60	5.66		8.77
	1κHz	7.60	7.58		8.45
FOD(0.20)	10Hz	7.19	7.33	18.0	13.02
	100Hz	11.19	11.52		19.30
	1κHz	15.19	15.21		17.06
FOD(0.25)	10Hz	8.99	9.08	22.5	17.01
	100Hz	13.99	14.26		23.80
	1κHz	18.99	19.01		20.13
FOD(0.30)	10Hz	10.79	10.73	27.0	20.75
	100Hz	16.79	16.95		28.21
	1κHz	22.79	22.63		24.27
FOD(0.35)	10Hz	12.59	12.42	31.5	25.10
	100Hz	19.59	20.01		32.56
	1κHz	26.59	26.46		28.84
FOD(0.40)	10Hz	14.39	14.18	36.0	29.85
	100Hz	22.39	22.60		36.55
	1κHz	30.39	30.13		33.18
FOD(0.45)	10Hz	16.18	15.91	40.5	34.40
	100Hz	25.18	25.54		41.04
	1κHz	34.18	33.83		37.70
FOD(0.50)	10Hz	17.98	17.99	45.0	39.29
	100Hz	27.98	28.13		45.45
	1κHz	37.98	37.68		41.28
FOD(0.55)	10Hz	19.78	19.64	49.5	44.48
	100Hz	30.78	31.10		49.65
	1κHz	41.78	41.31		44.87
FOD(0.60)	10Hz	21.58	21.35	54.0	49.36
	100Hz	33.58	33.58		52.60
	1κHz	45.58	45.09		48.41
FOD(0.65)	10Hz	23.38	23.40	58.5	54.36
	100Hz	36.38	36.69		56.61
	1κHz	49.38	49.14		50.74
FOD(0.70)	10Hz	25.17	24.84	63.0	59.50
	100Hz	39.17	39.09		60.63
	1κHz	53.17	52.51		52.01
FOD(0.75)	10Hz	26.97	26.58	67.5	65.02
	100Hz	41.97	41.55		64.64
	1κHz	56.97	55.62		51.69
FOD(0.80)	10Hz	28.77	28.31	72.0	70.19
	100Hz	44.77	44.51		67.91
	1κHz	60.77	59.22		48.64
FOD(0.85)	10Hz	30.57	30.76	76.5	74.95
	100Hz	47.57	47.23		70.51
	1κHz	64.57	62.10		41.63
FOD(0.90)	10Hz	32.37	33.95	81.0	79.31
	100Hz	50.37	51.50		71.42
	1κHz	68.37	64.69		29.52

Transient response of the design was also tested and analyzed. Sinusoidal input signal was used to clearly show the delay or the phase shift between the input and output signal. Transient response of FOD(0.25) is shown in Figure 11 for an input signal, where the frequency was set to 60Hz. At 60-Hz frequency, the magnitude gain of the FOD should be at $|G(j\omega)|_{\omega=2\pi f} = \omega^{0.25}|_{\omega=2\pi(60)} = 4.41$. Using the computed gain, with an input signal amplitude of 5mV, the output signal amplitude should then be equal to 22.03mV. This is close to the graph showing an output peak voltage of 22.16mV. Meanwhile, the time delay between two sine waves is equal to 1.03ms. The phase shift of the output signal with respect to the input signal is equal to 22.25°, which is close to the ideal phase angle for FOD(0.25) of 22.5°.

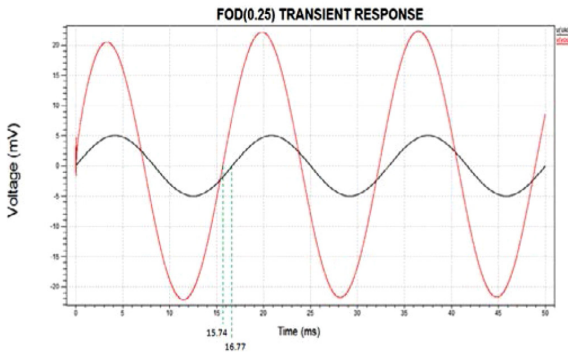

Fig. 11. FOD(0.25) transient response

V. OTHER DESIGN CONSIDERATIONS

Initial value of R_1 was carefully assessed. Using the computations in Table 1, R_1 value must be high to have capacitor values relatively smaller. Figure 8 shows that almost 95% of the total chip area is consumed by capacitors. However, it was also taken into consideration that other capacitance in the RC ladder must not fall down to tens of picofarad range, which is foreseen to be highly sensitive to parasitic capacitances.

The type of the capacitor implemented in this design was carefully chosen. NMOS-type of capacitor was considered in the study since it has higher capacitance value compared to poly-to-poly capacitor. Shown in Figure 12 is the comparison between the two types of capacitor. With regards to resistor, a poly type resistor was chosen for this study.

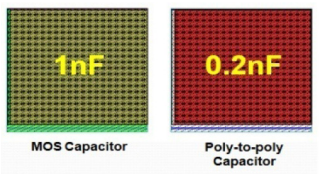

Fig. 12. Comparison of capacitance value of MOS and poly-to-poly capacitor having same physical dimension

T-gates characterization was done to examine the parasitic effects of the switches to the overall design. The number of t-gates in parallel has a significant effect to the phase response of an FOD. As a result, a 4-TG switch was used in the design to give a better phase response with the least physical dimension layout of the switch as possible. Shown in Figure 13 is the result of t-gate characterization.

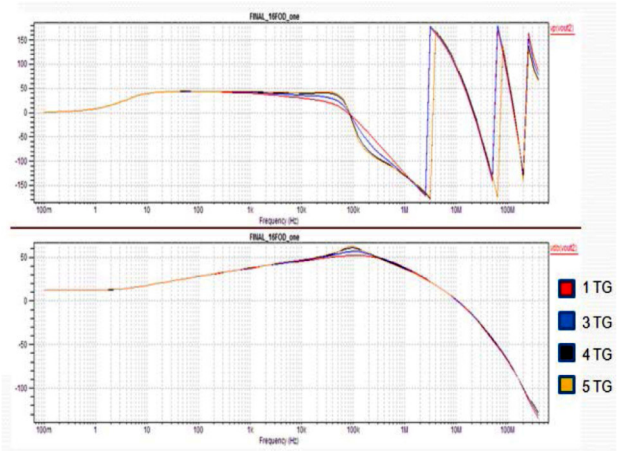

Fig. 13. Phase and gain response of an FOD for a switch with increasing number of transmission gate (TG)

VI. CONCLUSIONS

In this study, a design of a low-voltage selectable sixteen fractional-order differentiator (***0.10, 0.20, 0.25, 0.30, 0.35, 0.40, 0.45, 0.50, 0.55, 0.60, 0.65, 0.70, 0.75, 0.80, 0.85, and 0.90)*** has been designed and implemented in a microelectronic scale using 0.35um technology. Unlike in [16] which uses microcontroller for switching purposes, this design is successfully realized in an analog microelectronic scale, and thus, relatively smaller. The design employed reusability of capacitors and resistors when switching from one order to another. The final physical layout of the design using L-Edit has a dimension of 11.55mm x 8.32mm or equivalent to 96.10mm^2, which is just about three times the area of a semi-differentiator in [17]. The whole chip was powered using 1.5 Volt supply. Several design considerations such as the type of capacitor and resistor to implement, transmission gate design, and the initial value of R_1 were evaluated. The overall design was characterized in its frequency response —the magnitude and phase response for every order. The gain-bandwidth limitation of the op-amp actually bounds the frequency response of the 16FOD which opens up for possible research study in the future.

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REFERENCES

[1] IB. Ross, "The development of fractional calculus 1695–1900," *Historia Mathematica*, vol. 4, iss. 1, 1977, pp 75–89.

[2] Gonzales, E. (2013). *Design of robust fractional-order control systems*. Dissertation, PhD in ECE, De La Salle University, Manila, Philippines.

[3] I. Petras, D. Sierociuk, and I. Podlubny, "Identification of parameters of a half-order system," *IEEE Transactions on Signal Process.,* vol. 60, iss. 10, 2012, pp. 5561–5566.

[4] L. Dorčák, J. Valsa, J. Terpák, P. Horovčák, and E. Gonzalez, "Modeling and identification of fractional-order dynamical systems," *Proceedings of the 11th International Multidisciplinary Scientific Geoconference (SGEM2011)*, Jun. 20–25, 2011, Bulgaria, pp. 553–560.

[5] L. Dorčák, "Numerical models for simulation of the fractional-order control systems," The Academy of Sciences, Institute of Experimental Physics, UEF-04-94, Technical University of Koˇsice, Slovakia.

[6] M. Axtell and M. E. Bise, "Fractional calculus applications in control systems," *Proceedings of the IEEE 1990 National Aerospace and Electronics Conference*, May 21–25, 1990, New York, pp. 563–566.

[7] R. S. Barbosa, J. A. T. Machado, and I. M. Ferreira, "PID controller tuning using fractional calculus concepts," *Fractional Calculus & Applied Analysis*, vol. 7, no. 2, 2004, pp. 119–34.

[8] J. A. T. Machado, "Analysis and design of fractional-order digital control systems," *Journal of Systems Analysis, Modeling and Simulation*, vol. 27, 1997, pp. 107–122.

[9] R. Magin, M. Ortigueira, I. Podlubny, and J. Trujillo, "On the fractional signals and systems," *Signal Processing*, vol. 91, iss. 3, Mar. 2011, pp. 350–371.

[10] W.M. Ahmad and K. Assaleh, "Modeling of speech signals using fractional calculus," *9th International Symposium on Signal Processing and Its Applications*, 2007, pp. 1–4.

[11] A. Oustaloup, "Fractional order sinusoidal oscillators: optimization and their use in highly linear FM modulation," *IEEE Transactions on Circuits and Systems*, vol. CAS-28, no. 10, Oct. 1981.

[12] Biswas, K., Sen, S., and Dutta, P.K. (2006). Realization of a coznstant phase element and its performance study in a differentiator circuit. IEEE Transactions on Circuits and Systems, 53 (9), pp. 802–806.

[13] Sheng, H., Sun, H., Coopmans, C., Chen, Y., and Bohannan, G. (2010). Physical experimental study of variable-order fractional integrator and differentiator. IFAC Workshop Fractional Differentiation and Its Applications, 4, pp 1–6.

[14] Jiang, C.X., Carletta, J.E., and Hartley, T.T. (2007). Implementation of fractional-order operators on field programmable gate arrays. Advances in Fractional Calculus, pp. 333–346.

[15] Valsa, J., Dvořák, P., and Friedl, M. (2011). Network model of the CPE.Radio Engineering, 20 (3), pp. 619–626.

[16] Gonzalez, E.A., Dorčák, L., Monje, C.A., Petráš, I., and Valsa, J., Caluyo, F.S., Gonzalez, R.M., Jundez, C.P.M., Reyes, D.D., & Villanueva, T.M.G. (2014). Conceptual design of a selectable fractional-order differentiator for industrial applications. Fractional Calculus and Applied Analysis, 17 (3), pp. 697–716.

[17] A. C. Abad, E. A. Gonzalez, R. Y. Yap, and L. Dorcak (2014, January 02). Analog realization of a fractional-order element on 0.35 um CMOS technology [Online]. http://vixra.org/pdf/1401.0016v1.pdf

[18] Abulencia, G. L. and Abad, A. C., Analog realization of a low-voltage two-order selectable fractional-order differentiator in a 0.35um CMOS technology, International Conference on Humanoid, Nanotechnology, Information Technology,Communication and Control, Environment and Management (HNICEM), Cebu, Philippines, 2015

[19] Podlubny, I., Petráš, I., Dorčák, L., Vinagre, B.M., and O'Leary, P. (2002). Analogue realizations of fractional-order controllers. Nonlinear Dynamics, 29, pp. 281–296.

[20] R. Yap and W. Y. Chung, "A 1.2V Reduced Output Reference Voltage Bandgap," Proceedings of the 10th DLSU Science & Technology Congress, July 23, 2008, De La Salle University–Manila.

[21] Yap, Roderick, "A Low Voltage Dynamic Power Saving Pulse Frequency Modulated Boost Converter Design for Driving a White LED", MS Thesis Document, Chung Yuan Christian University. Taiwan, January 2009.

[22] Allen, P. and Holberg, D. (2002). CMOS analog circuit design. New York: Oxford University Press.