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# CMOS Implementation of Hysteretic Controller for a DC-to-DC Buck Converter using 0.35um Library

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**Abstract:** Hysteretic comparators employ positive feedback mechanism which would enable the system to constantly check whether the output exceeds the lower and upper threshold voltages. By applying this system to a DC to DC buck converter, the use of Pulse Width Modulated (PWM) signals would not be necessary anymore when the circuit has stabilized after it is turned on. In this research, a 3.3V input was stepped down to a 1.5V output with a minimum current of 10mA. A start-up circuit using XOR and XNOR gates were used to provide initial pulses from 0us to 100us to ensure that the buck converter can initially charge up and provide a change in the negative input of the comparator. An op-amp based Reference bandgap voltage was also included in the design and was placed at the positive input terminal of the comparator. Testing was done on all process corner libraries and the output showed consistency, having only minimal deviations. Temperature sweep from 25°C to 80°C, line regulation from 2.9V to 3.3V, and load regulation from 100Ω to 500Ω were also checked. The output for load regulation ranged from 1.5038V to 1.5903V for a 100Ω load, and 1.5239V to 1.6204V for a 500Ω load. The output voltage of the buck converter ranged from 1.2V to 2V thereby producing an average of around 1.5V. The final layout had a size of 1499.05um x 1056.1um.

**Key Words:** Buck Converter; CMOS; DC-to-DC; Hysteresis; 0.35um Library

## 1. INTRODUCTION

A buck converter is a device which steps down an input DC voltage. With an open loop, a buck converter would have a bad regulation in its load and line (Sengupta, 2007). To improve the system, a controller or comparator is implemented in the buck converter.

Many available comparators used in DC-to-DC converter nowadays vary from one another in terms of their functions and characteristics. These different designs experience different problems which could influence the overall circuit. These problems include: (1) uncertainty on whether the output would reach a value near the supply rails, (2) slow switching time and transition time thereby affecting the output especially if the circuit has varying inputs, (3) noise may unexpectedly come up and interrupt the signal, which could then cause an effect to the waveform, and (4) there is a possibility for unwanted transitions to occur (Moghimi, 2000). Designing the controller circuit for a DC to DC converter in CMOS can pose a lot of challenges when

it comes to circuit components. To name a few, monitoring the output may need error amplifiers (Chua-Chin Wang, 2011) (Yeong-Tsair Lin, 2007). Others have Analog to Digital converters (Xiao, 2004)(Wang Kun, 2006). Some converters make use of comparators in lieu of analog to digital converters (Islam, 2004). Alternatively, a hysteretic comparator can be a simpler approach to lessening the circuit complexity if one is not too particular about output ripples.

Among the many techniques in improving a DC-to-DC converter, the usage of a Hysteretic controller can be further researched. A Hysteretic controller is a bistable multivibrator. They are known for employing a positive feedback mechanism which eliminates noise that can be incurred due to the input signal. Focusing on the application of a DC-to-DC converter which steps down a given voltage, it is possible to utilize operational amplifiers in order to design the overall converter using a hysteretic comparator (Chauhan, 2014). This comparator enables fast transient response and stable operation of a given circuit. To fully appreciate the essence of utilizing a hysteretic comparator in DC-to-DC buck conversion, an integrated circuit design of a hysteretic controller in DC-to-DC buck conversion was done using CMOS technology. The usage of CMOS enables low power dissipation but speed is a limiting factor (Madhavan, 2012).

## 2. METHODOLOGY

In achieving the design, a modular systematic way is implemented. The main objective is to be able to implement a hysteretic controller in a buck converter using a 0.35 um CMOS library. The designs are based on different sources and have been improved to create a better overall circuit functionality. Different related literatures such as textbooks and past researches regarding the DC-to-DC buck converter and the hysteretic controllers were gathered and the significant sources were filtered out. This paved way for the framework of the circuit design. The design is divided into 4 parts for faster troubleshooting. The 4 main parts are as follows: (1) DC-to-DC buck converter, (2) Hysteretic Controller, (3) Start-up circuit, and (4) bandgap design. The operational amplifier implemented was a Two-Stage CMOS Op-Amp (Allen & Holdberg, 2002). The computations, however, are based on the needed specifications in the design. There are 4 hierarchical stages implemented in the design process - discrete component level, MOS design level, Spice design level and IC layout level.

### *2.1 Computation*

The design of the buck converter and the hysteretic controller needed computations to be able to get an output based on the specifications. The first one computed are the resistor, capacitor, and the inductor of the buck converter. The computations were based on having a duty cycle of 45.45% and having a ripple of 0.5%. Another part of the circuit that needed computations was the hysteretic controller.

### *2.2 Discrete Component Level Process*

The characteristics and behavior of each circuit was identified through the simulations. The first simulated circuit was the buck converter with the hysteretic controller and start up circuit. Afterwards, each of the circuits was analyzed individually to see if they are working correctly. The start-up circuit and the bandgap circuit were based on previous researches. A way was found to create an original circuit diagram. It is important to make sure that the desired operating parameters are achieved before continuing the design. Testing equipment like oscilloscope and digital multimeter, and analogue analysis are used to evaluate the result.

As seen in Fig. 1, mechanical switches are employed in the simulation to see if the hysteretic controller is the one responsible in creating the output or not. This mechanical switch is removed in future simulations. The initial testing showed that the computations done were right and the desired output was obtained.

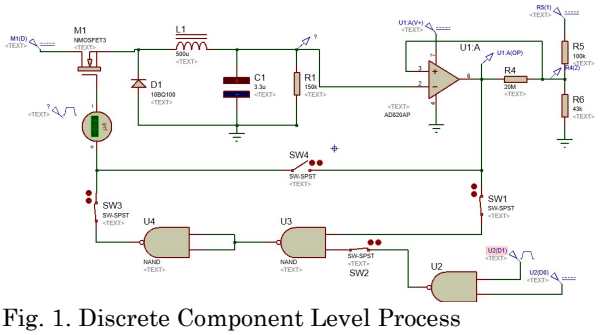


Fig. 1. Discrete Component Level Process

After ensuring the simulation is completely working, innovation of the design was done by optimizing the number of components and testing the modified circuit for next design level.

### *2.3 MOS Design Level*

Ensuring everything works perfectly, the discrete components were converted into MOS transistor level as shown in figure 2. This will serve as the schematic diagram for the coding in spice netlist level. Multisim was used to CAD the design. All the specifications were accurately labeled in the schematic diagram. Furthermore, node names were added in preparation for SPICE coding.

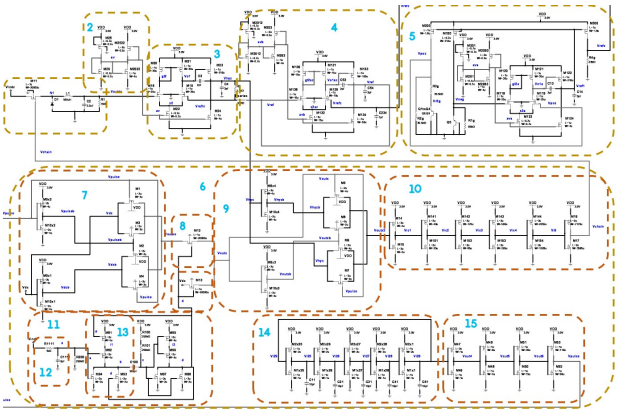

Fig. 2. MOS Design Level

## 3. RESULTS AND DISCUSSION

### *3.1 Hysteretic Comparator Testing*

The target deadband set was 300mV minimum. This was set in a way that would allow the output ripple to pass through the upper and lower threshold values.

Two tests were conducted to see the behaviour and obtain the deadband as seen in figures 3 and 4. For the first test, a triangular wave was used as an input. The purpose of doing so is to determine the upper and lower thresholds of the circuit, as well as the deadband. The hysteretic comparator triggered beyond the threshold values found in the test are 1.21 V and 1.727 V. Another test used a noisy sine wave. It ranges from 0.8V to 1.8V and was found to trigger at 1.22V and 1.71V. The target deadband was met as the deadband obtained was 500mV.

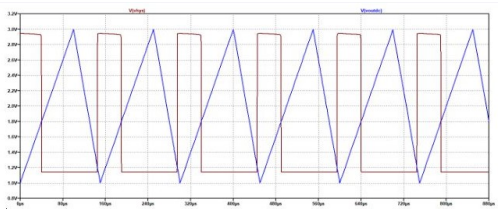

Fig. 3. Hysteretic Controller Testing 1

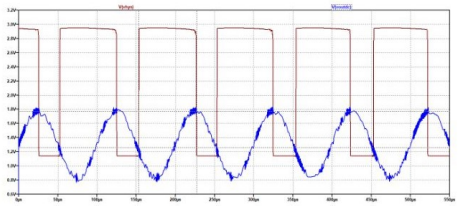

Fig. 4. Hysteretic Controller Testing 2

3.2 Whole Circuit Testing

The outputs observed were the output voltage of the buck converter, the current flowing through the load, and the output of the hysteretic comparator. Figure 5 shows output simulation result. Each corner library was simulated and the results are summarized in Table 1. It can be observed that at TT, FF, and FS corner libraries, the output voltage from the converter deviates only a little from the ideal value of 1.5V.

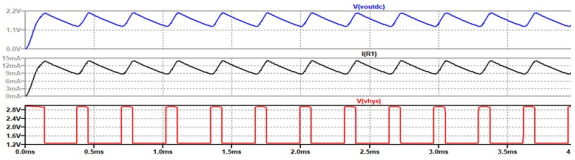

Fig. 5. Sample Simulation

On the other hand, when the circuit is operating at SS and SF, the output voltage is relatively higher. It can be deduced that the operation of the NMOS would have a greater influence in the overall design. Thus, by having a faster NMOS, a better output can be obtained. The worst case scenario is observed in SS. This is likely so because both transistors are slow. For the current values, all libraries exceed the minimum current value of 10mA. Additionally, the frequency from the hysteretic comparator is relatively slower than that of the other converters, ranging from 3 kHz to 3.4

kHz. This is likely so because the operation of the converter is dependent on the output of the buck converter.

Table 1. Whole Circuit Test Result

| Corner Library | Output Voltage (V) | Output Current (mA) | Frequency (kHz) |
|---|---|---|---|
| Typical-Typical | 1.5006 | 10.004 | 3.4621622 |
| Fast-Fast | 1.5067 | 10.044 | 3.3710526 |
| Slow-Slow | 1.5525 | 10.350 | 3.0212264 |
| Slow-Fast | 1.5428 | 10.285 | 3.0500000 |
| Fast-Slow | 1.5038 | 10.025 | 3.4069149 |

### *3.3 Temperature Sweep Testing*

Temperature testing was done at room temperature of 25°C, and at a hot temperature of 80°C. This is shown in Tables 2 and 3. Based on the output obtained, it can be seen that the voltage variation is still within 10% of the desired output voltage. This value is acceptable since it is assumed that the circuit would not reach this high temperature. It can also be observed that the frequency for TT, FF, and FS increased, while the opposite happened to SS and SF. Thus, circuit operation is mostly dependent on the NMOS transistor. Additionally, it can be observed that although the temperature changes, the amount of current flowing through the load does not go below the minimum value of 10mA.

Table 2. 25°C Temperature Sweep

| Corner Library | Output Voltage (V) | Output Current (mA) | Frequency (kHz) |
|---|---|---|---|
| Typical-Typical | 1.5006 | 10.004 | 3.4621622 |
| Fast-Fast | 1.5067 | 10.044 | 3.3710526 |
| Slow-Slow | 1.5525 | 10.350 | 3.0212264 |
| Slow-Fast | 1.5428 | 10.285 | 3.0500000 |
| Fast-Slow | 1.5038 | 10.025 | 3.4069149 |

Table 3. 80°C Temperature Sweep

| Corner Library | Output Voltage (V) | Output Current (mA) | Frequency (kHz) |
|---|---|---|---|
| Typical-Typical | 1.5333 | 10.222 | 3.4809783 |
| Fast-Fast | 1.5168 | 10.112 | 3.4435484 |
| Slow-Slow | 1.6018 | 10.679 | 3.0212264 |
| Slow-Fast | 1.5862 | 10.575 | 2.859375 |
| Fast-Slow | 1.5135 | 10.09 | 3.4809783 |

### *3.4 IC Layout*

Layout was done through the use of L-edit. This program has the ability to perform parasitic extraction thereby allowing a more realistic performance analysis. The overall design can be seen in Figure 6. Two op amps were used in the design. The first has bigger sizes and a better gain, while the second one has smaller sizes and a better unity gain bandwidth. Thus, the first op amp was used for the hysteretic comparator while the second one was used for the voltage follower from the reference to the hysteretic comparator. Figures 7 to 10 show the IC layouts of the different blocks comprising the design. In figure 10, the layout of the BJT is purposely not shown.

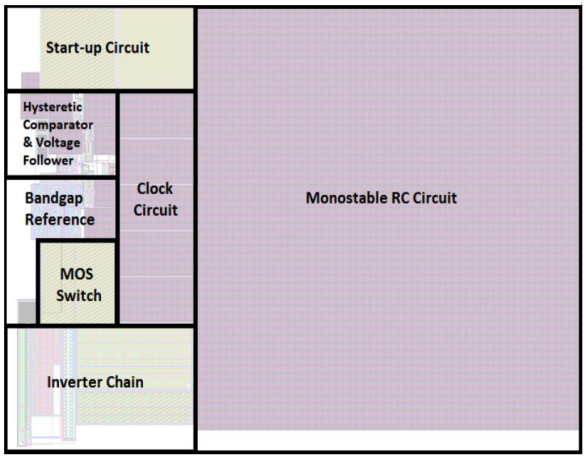


Fig. 6. Project Layout

### *3.5 Monte Carlo and Worst Case Analyis*

The final test done to the circuit is using Monte Carlo Analysis. Since Slow-Slow consistently has the worst performance, the test was performed only at this corner library for reliability. The voltage supplied is stepped within 10% of 3V, the temperature sweep was from 25°C to 80°C, and the switching speed of MOS transistors was varied by 3 Sigma deviations. The result shows that the hysteretic controller triggered at different speed.

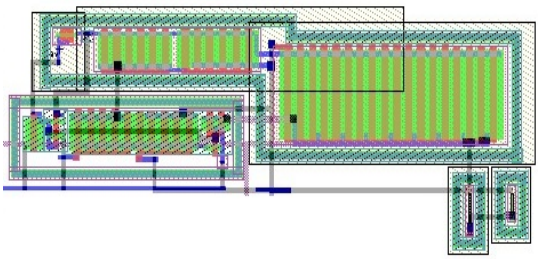

Fig. 7. Hysteretic Comparator Layout without Capacitors

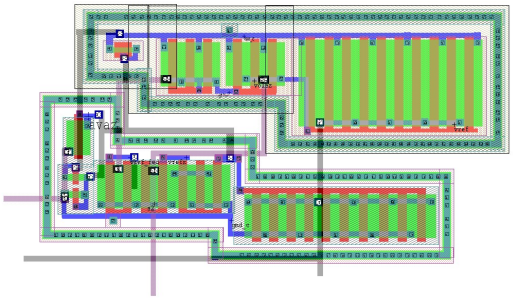

Fig. 8. Voltage Follower Layout without Capacitors

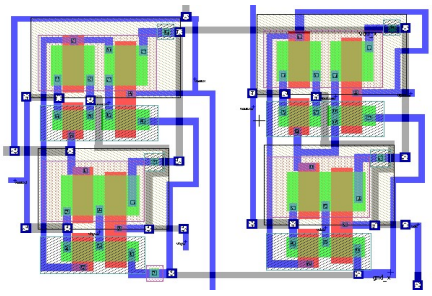

Fig. 9. Start-up Circuit Layout without switches

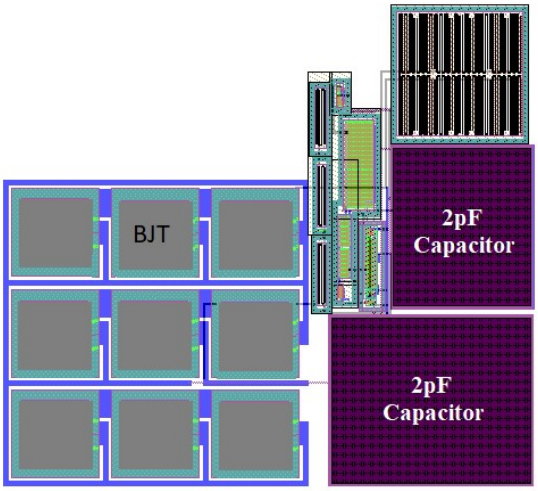


Fig. 10. Bandgap Reference Layout

## 4. CONCLUSIONS

The research focused on using a Hysteretic comparator designed to supply pulses for the switch of a DC to DC buck converter and implementing it using the 0.35um library. A system comprising of the DC to DC step down converter, Hysteretic comparator, Bandgap Reference, Voltage Follower, Start-up circuit, and a monostable multivibrator were designed and implemented using Tanner. The pre-layout and post-layout simulations were tested in all corner libraries and the output voltages had an average value of 1.55V, with currents ranging from 10mA to 10.8mA. Temperature sweep, load regulation, and line regulation were also tested and the results proved to be positive. For the load regulation, it was observed that for a load resistance of 100 ohms, the output ranged from 1.5038V to 1.5903V. For a load resistance of 500 ohms, the output ranged from 1.5239V to 1.6204V. The output characteristics of the system were compared to that of other studies involving dc to dc converters, as well as references of the hysteretic comparator.

Overall, the comparator designed in this paper has shown a faster settling time as compared to other works done in the university such as the DC to DC boost converter using posicast controller (Chua et al., 2013), CMOS based low voltage PWM boost converter (Cabrera, 2010,) and a fully integrated all-digital reduced capacitor controller for a DC to DC boost converter (Castillo et al., 2015). In terms of the

circuit size, the work of (Castillo et al., 2015) has a smaller dimension due to its capacitor-less design, as compared to the comparator designed in this research paper. However, among the related literature, only the work of (Castillo et al., 2015) has presented a circuit size, thereby limiting the material used for comparison in terms of circuit size.

Further research is recommended to utilize other means of making a hysteretic controller, such as using SR Flip flops so that comparisons can be made on which of these would produce better results. In addition, it is also recommended that future researchers study the systematic implementation of global and local Monte Carlo in testing the output and performance of the design.

## 5. ACKNOWLEDGMENTS

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