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Random Channel Generator for PLC Channel Emulator

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Abstract: PLC channel emulator is an important piece of hardware that allows stress testing of existing and newly developed PLC modems instead of directly connecting it to the energized power lines. This does not only save money and time, it also allows repetition of the same test in order to develop a more robust modem design. Various power line measurements, models, and transfer functions have been conducted and show that the power line is not only a hostile environment, it also periodically varies. The variation is due to several factors which include change in the physical topology, plugging in and out of loads, switching on and off of appliances and electronic devices, and even the time of day. To test the PLC modem with these variations without the hazard of the actual energized line, a PLC channel emulator that contains channel variates is developed. The channel variates are generated by means of a random channel selector which switches the channel from one variate to another.

Key Words: PLC; PLC channel emulator; random channel generator; PLC modem; FPGA

1. INTRODUCTION

PLC Channel emulator is a device that mimics the characteristics of the power lines. Its main purpose is to test PLC devices particularly transceiver. The power lines are intended for power delivery, thus, when used as a communications channel, it proves to be hostile to the communications signals (Liu, Bumiller, & Gao, March 2014). Nonetheless, the renewed interest in PLC related researches spawned from the idea of the Smart Grid, which allows the power lines to act as a communications medium while delivering power.

The random channel generation is a feature in the PLC channel emulator that allows it to change the behavior of the channel randomly and automatically, thus, mimicking a real power line network. Doing so would allow designers to redesign their PLC devices to make them more robust to these variations. Testing the PLC devices on actual live networks is costly and non-repetitive making it difficult to determine the cause of the problem. Current channel emulators also utilize random channel generation of PLC channels but they are being handled by computers and not as a standalone device like FPGA (Liu, 2013) and (Gotz,).

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2. METHODOLOGY

The random channel generator (RCG) is an FPGA block that generates the channel to which the signal is passed to. It comprises of a random number generator (RNG), multiplexer and the channel transfer functions (CTF) (Fig. 1). The RNG is implemented using a modified linear feedback shift register (LFSR). LFSRs are easily implemented using simple exclusive OR logic gates for the taps and D-type flip flops for the shift register (Lv, Fang, Xie, & Qi, 2012). By performing left shift and XOR operations, and tapping it on specific points, a random number is generated. In this study, the RNG developed uses a 32-bit vector with only 3 taps. Fig. 2 shows the logic circuit.

Initially, the RNG needs a constant state to generate succeeding values. This is done through simultaneously shifting of the register and performing the XOR operation for the taps (Saluja, 1991). The initial value can be mathematically represented as shown on Eqn. 1 and referred to as the seed.

$$Reg = [X0(Bit\ 31\ to\ Bit\ 0)] \quad \text{(Eq. 1)}$$

where

Reg = 32 bit vector register and
X0 = 32 bit seed

The series of vectors produced by the RNG are pseudo-random, meaning, the vectors possess the statistical property of randomness but not entirely random. This is because the values are only repeating in powers of 2. Thus, the values or the intervals can be computed using Eqn. 2.

$$\text{Interval} = 2^n - 1 \quad \text{(Eq. 2)}$$

In a truly random sequence, it should be occurring in varying intervals. Therefore, by making use of a maximum length sequence generator (MLSG) with k number of taps, better randomness can be achieved.

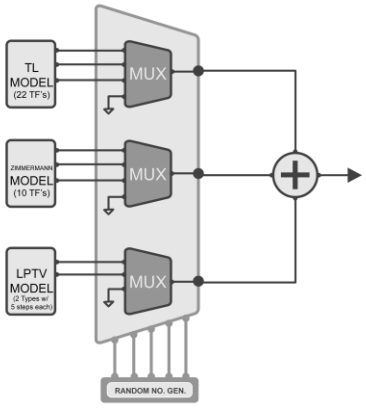


Fig. 1. Random Channel Generator

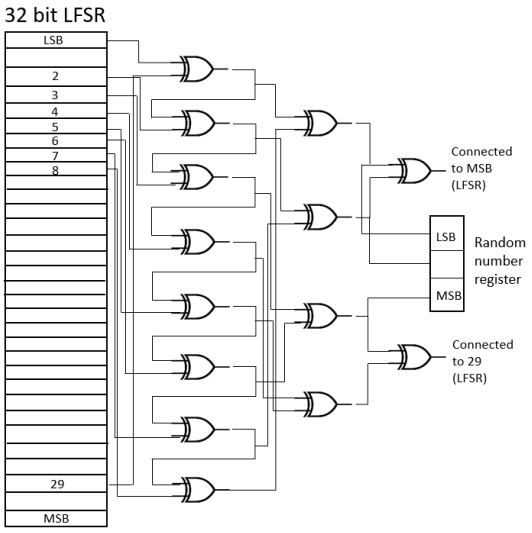
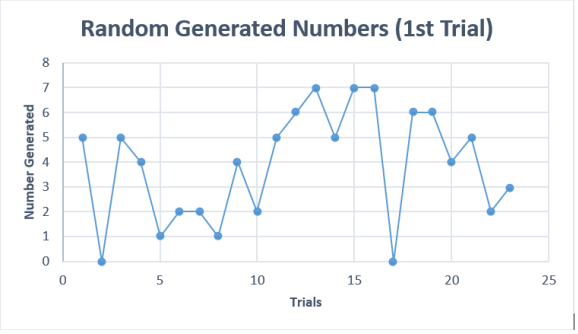


Fig. 2. Random Number Generator using LFSR

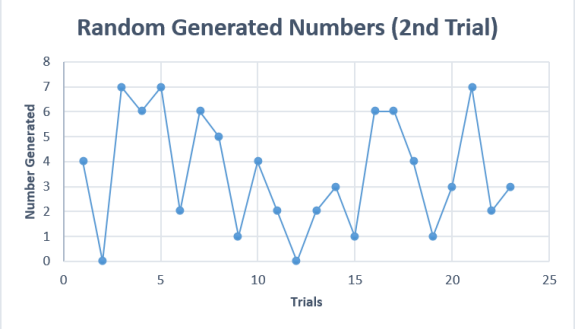
The 3-bit output of the random number generator is connected to the multiplexers that would choose what channel models will be selected. The above is implemented on Kintex-7 board.

3. RESULTS AND DISCUSSION

Test results for the random number generator are shown on Fig. 3. Two trials are done to see if a pattern occurs. Both trials use up to 24 cycles and for each cycle, an external user interface (UI) is used to determine the periodicity of the RNG. For each press of the UI, the number generated is logged. Both trials attest the randomness of the RNG.



(a) Trial 1



(b) Trial 2

Fig. 3. Periodicity of the Random Number Generator

Another metric used to determine the randomness of the RNG is the distribution. The Verilog code for the LFSR is run to generate one thousand (1000) numbers and saved in a .csv file. The histogram is then plotted in Excel and the chart is shown in Fig. 4.

The 3-bit LFSR generates the numbers 0 to 7 and is represented in the x-axis. The y-axis shows the number of times the number showed up. The chart shows an almost uniform distribution.

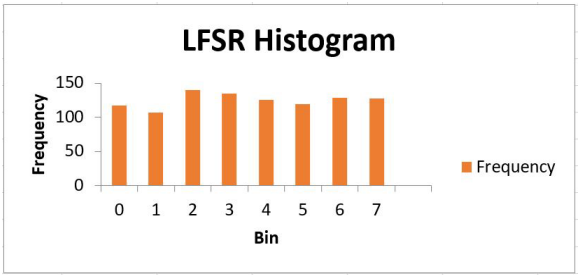


Fig. 4. RNG Histogram of the LFSR

4. CONCLUSIONS

The development of the random number generator for PLC channel emulator was successfully implemented on Kintex-7 FPGA. The performance of the RNG was evaluated and showed a uniform distribution. The random nature of the RNG allowed the generation of random PLC channels which is a realistic PLC channel scenario. The RNG is used to generate actual channel transfer functions based on three models, the Transmission line model (TL) (Canete, et.al, Dec. 2011), the multipath model first tackled by Zimmermann (Zimmermann & Dostert, April 2002), and the linearly periodically time varying (LPTV) model (Canete, et.al. Nov. 2008). While the RNG developed here generated random channel scenarios, the different loading conditions caused by the appliances and other electrical loads connected to the power line are not considered. It was noted in one of our characterization of the power line that switching on and off of appliances greatly affect the transmission. Thus, the electrical loads affect the behavior of the power line and their effects depend on the type of the load. Since the usage of the appliances vary, there are those that are used more often than others, it is best to categorize the loads according to their probability of usage. A random number generator that will consider the weighted probability of occurrence of the electrical loads is recommended for future work.

5. ACKNOWLEDGMENTS

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6. REFERENCES

Canete, F. J., Cortes, J. A., Diez, L., & Entrambasaguas, J. T. (Dec. 2011). A channel model proposal for indoor power line communications. *IEEE Communications Magazine*, (pp. 166–174).

Canete, F., Diez, L., Cortes, J., Sanchez-Martinez, J., & Torres, L. (Nov. 2008). Time-varying channel emulator for indoor power line communications. *Global Telecommunications Conference 2008* (pp. 1-5). IEEE GLOBECOM 2008.

Gotz, M. and Dostert, K. (2002) "A universal high speed powerline channel emulation system," in Broadband Communications, 2002. Access, Transmission, Networking. 2002 International Zurich Seminar on, pp. 24–1–24–6.

Liu, W., Bumiller, G., & Gao, H. (March 2014). On (power-) line defined plc system. *18th IEEE International Symposium on Power Line Communications and Its Applications*, (pp. 81-86).

Liu, W. (2013) Emulation of Narrowband Powerline Data Transmission Channels and Evaluation of PLC Systems. PhD thesis, Karlsruher Instituts f¨ur Technologie.

Lv, H., Fang, J., Xie, J. X., & Qi, P. (2012). Generating of a nonlinear pseudorandom sequence using linear feedback shift register. *2012 International Conference on ICT Convergence (ICTC).* Jeju Island.

Saluja, K. (1991). *Linear feedback shift registers theory and applications.* Madison: University of Wisconsin.

Zimmermann, M., & Dostert, K. (April 2002). A multipath model for the powerline channel. *Communications IEEE Transactions on*, (pp. 553-559).