Presented at the Research Congress 2013
De La Salle University Manila
March 7-9, 2013

RFID-BASED AUDIO AND TEXTUAL GUIDE FOR MUSEUMS

Earl Shawn Ang [1] , Cyril Albert Enriquez[2], and Paolo Neil Posadas [3] and Cesar Llorente [4]
[1,2,3,4] ECE Dept. Gokongwei College Of Engineering, DLSU

Abstract: Deployment of technologies that alleviates the effects of human fatigue and monotony can enhance the experience of visitors in the museums. Audio recordings can be played back repeatedly without deterioration brought about by fatigue and boredom. Such technologies based on Radio Frequency ID tags can be used to identify or tag an artifact. A recording or multimedia presentation can be associated to a particular tag. This presentation can be activated or played back in a portable device when it detects the tag. The portable device is carried by the tour guide. In this study, a portable device is developed to scan or detect an RF tag and play back an audio recording describing the artifact. It utilizes the NIOSII softcore processor and implemented on Altera Corporation's DE2 FPGA Development Board using Quatus II SOPC Builder. Tests showed that the system is able to detect the tag placed in the artifact and played back the corresponding wav audio recording with 100% accuracy.

Key Words: NIOS II softcore processor; RFID –activated audio recording; DE2 embedded system; Nios II Embedded Suite (EDS); SOPC Builder

1. INTRODUCTION

Museums provide repositories of a nation's cultural heritage . They provide very rich source of information reflected and embodied on various artifacts that provided a record of the history of a nation or people. Going to a museum is a very enriching experience. A major factor to the quality of the experience is on the presentation of the artifacts, how they are arranged and presented, and how complete the information provided by tour guides, who normally accompany the visitors.

The quality of presentation is greatly affected by factors such as the size of the group, the disposition of the guides, and environmental factors within the museums. As the repetition of the presentation normally brought about by several number of tour groups, the quality of presentation of the guides pertaining to the artifacts are affected, increasing the possibility of missing out information. There are deployment of technologies that aim for richer museum visit experience (Tesoriero, R. et.al, 2008). A portable devices such as a PDA provide information indicated by the tag associated to a museum piece. However, not all patrons in the museum have access to mobile devices such as PDAs

In this study, a portable device is developed to scan or detect an RF tag and play back an audio recording describing the artifact. The goal of the study is to develop a portable hand-held device that can play back recordings when activated by an RF ID tag. For the embedded microcomputer system, the NIOSII softcore processor (Altera, 2009) was used and integrated

using the SOPC Builder (Altera, 2009). Hardware interfacing logic were developed in Verilog Hardware Description language using Quartus II. Software development is with the C programming language.

2. METHODOLOGY

The methodology employed is developmental where the embedded system hardware is synthesized using the SOPC Builder of the Quartus II Electronic Design automation software (Altera, 2009). NIOS II softcore processor was selected as the main processor of the embedded system. Interface logic that includes the SRAM and SDRAM IP Core controller interfaces, the SPI controller, Audio DAC FIFO and other interface glue logic were synthesized in Verilog using the SOPC Builder Tool. For each Verilog module developed, a test fixture is also developed to test the functionality of the module, before integrating the whole system. The synthesized embedded hardware is downloaded to Altera's DE2 FPGA Development Board.

The C program is then developed using the Nios II Embedded Suite (EDS). For this study, ten artifacts were considered. An RF ID tag is to each artifact and an audio recording describing the artifact is associated to the tag. The recording is stored in the Compact Flash Memory card. In order to manage the complexity of the design and its implementation, each synthesized component are tested with the associated test fixture.

Testing the system, involves downloading the NIOS II softcore processor-based embedded system and the associated C language program into the DE2 FPGA Development Board (Altera, 2010). The RFID ID tags are placed near the RFID tag reader. The code for each RFID tags are then checked to ensure that each tag is in good condition. The distance between the reader and the tag resulting to playback of the audio recording is then measure. Tests are also carried out using different positions of the tag with respect to the reader that will still ensure correct reading of the tag.

3. RESULTS AND DISCUSSION

Figure 1 shows the system block diagram. Interfacing the RFID reader to the DE2 FPGA Development Board required an RS232C level converter to be inserted between the RFID reader and the DE2 board since the output generated by the RFID reader is not RS232C level. All other components are built-in to the DE2 board.

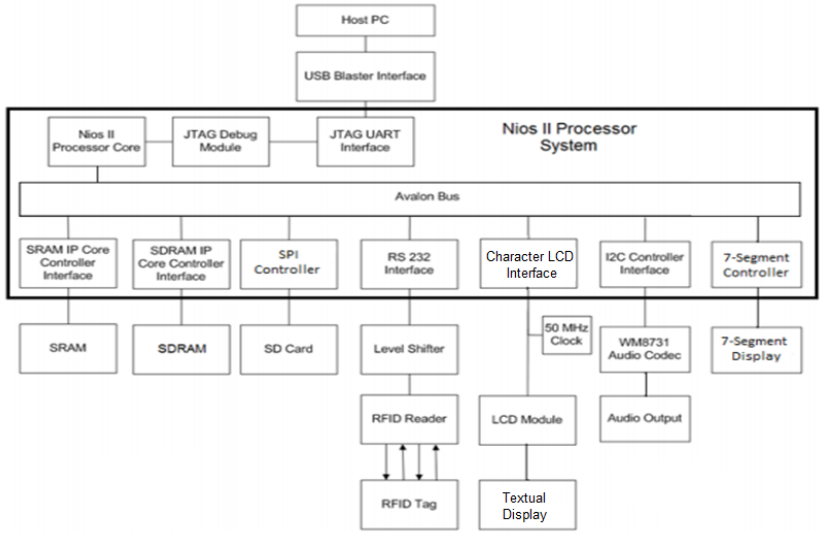

Figure 1. Block diagram of the RFID-based Audio and Textual Guide for Museum.

Based on the compilation results, the total logic elements of the Cyclone II FPGA consumed by the hardware design amounts to 6842 LEs. The combinational functions consumed 5807 LEs while the logic registers amount to 3609 LEs. Total registers amounted to 3726. The total pins used were 425, 89% of the total 475. The memory bits utilized were 386560 which is 80% of the available 483840. This is shown in Figure 2 below.

Entity	Logic Cells	Dedicated Logic Registers	Memory Bits	M4Ks	LUT/Register LCs	I/O Registers	Pins	Register-Only LCs	LUT-Only LCs
Cyclone II: EP2C35F672C6									
DE2_SD_Card_Audio	6842 (1)	3609 (0)	386560	99	2574 (0)	117 (117)	425	1035 (0)	3233 (1)
SDRAM_PLL:PLL1	0 (0)	0 (0)	0	0	0 (0)	0 (0)	0	0 (0)	0 (0)
altpll:altpll_component	0 (0)	0 (0)	0	0	0 (0)	0 (0)	0	0 (0)	0 (0)
Audio_PLL:PLL2	0 (0)	0 (0)	0	0	0 (0)	0 (0)	0	0 (0)	0 (0)
altpll:altpll_component	0 (0)	0 (0)	0	0	0 (0)	0 (0)	0	0 (0)	0 (0)
sld_hub:auto_hub	134 (92)	68 (39)	0	0	56 (29)	0 (0)	0	13 (11)	65 (52)
Reset_Delay:delay1	33 (33)	25 (25)	0	0	25 (25)	0 (0)	0	0 (0)	8 (8)
pzdyqx:nabboc	119 (0)	72 (0)	0	0	67 (0)	0 (0)	0	5 (0)	47 (0)
system_0:u0	6384 (1)	3371 (0)	386560	99	2361 (0)	0 (0)	0	1010 (0)	3013 (1)
I2C_AV_Config:u1	172 (116)	73 (44)	0	0	66 (44)	0 (0)	0	7 (0)	99 (72)
I2C_Controller:u0	56 (56)	29 (29)	0	0	22 (22)	0 (0)	0	7 (7)	27 (27)

Figure 2. Summary of the FPGA resources used after the design is compiled.

The tags conditons are ascertained by connecting the RFID reader to a host PC using the Hyperterminal program. Figure 3 shows the screenshot of the hyperterminal window showing the RFID tag codes for the ten tags used in this study.

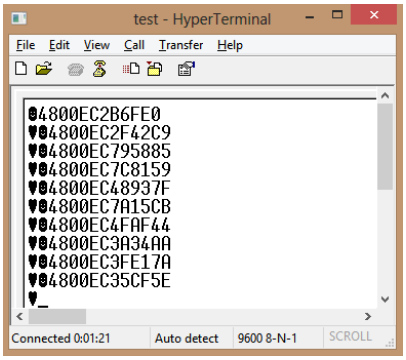

Figure 3. Screenshot of the hyperterminal window showing the RFID tags.

Testing the distances by which the tags can be properly detected by the readers under various positions of the tag relative to the readers is summarized in Table 1. Data show that the distance between the tag and the reader is maximum yielding correct reading is when its relative position to the reader is perpendicular.

Table 1. Tabulation of the distance between RFID tag andRFID reader under various relative positions that yield tag detection and correct reading.

Trial number	Distance, cm (tag parallel)	Distance, cm (tag perpendicular)	Distance, cm (tag parallel and beside the reader)	Distance, cm (tag perpendicular and beside the reader)
1	6.4	1.4	3.2	6.2
2	6.3	1.6	3.1	6.2
3	6.8	1.5	3.1	6.3
4	6.5	1.4	3.2	6.5
5	6.7	1.5	3.2	6.3
Average	6.54	1.48	3.16	6.3

The association of the wav files stored in the SD card is summarized in Table 2. Placing the tag in the reader caused the RFID reader to transmit the tag code to the NIOS embedded system. This code is looked up to the wav file in the SD card which is then sent to the Audio Codec for audio play via the I2C interface.

Table 2. Tabulation of the RFID tags and the corresponding wav recording file for playback.

RFID Card number	RFID tag code	RFID data Received by NIOS II	Audio File Accessed
1	4800EC2B6FE0	4800EC2B6FE0	Coronation of the Virgin Mary.wav
2	4800EC2F42C9	4800EC2F42C9	Retablo.wav
3	4800EC795885	4800EC795885	Spoliarium.wav

4	4800EC7C8159	4800EC7C8159	Mother and Child.wav
5	4800EC48937F	4800EC48937F	Governon Dasmarinas.wav
6	4800EC7A15CB	4800EC7A15CB	Harana in Manila.wav
7	4800EC4FAF44	4800EC4FAF44	La Descension de Jesus.wav
8	4800EC3A34AA	4800EC3A34AA	Bust of Mons G Aglipay.wav
9	4800EC3FE17A	4800EC3FE17A	Burning of Sto Domingo.wav
10	4800EC35CF5E	4800EC35CF5E	Christmas Card Series.wav

4. CONCLUSIONS

The Nios II Processor Embedded System interfaced to the external RFID reader and the internal components found in the Altera DE2 Board which includes the Cyclone II FPGA, SD Card Port, Wolfson WM8731 Audio CODEC Chip, RS232 Port, SRAM, SDRAM, and the 16x2 Character LCD, formed the complete RFID-based Audio and Textual Guide for Museum system. The master peripheral that was utilized was the Nios II Processor where the RFID data signal was processed for matching. The slave peripherals were the interfaces of the components mentioned above. The hardware design was developed by using the Quartus II software in which Verilog was used as the Hardware Design Language (HDL).

In order to create the whole hardware system, the System-On-A-Programmable-Chip (SOPC) Builder was utilized in order to construct the different hardware modules necessary for the construction of the thesis. The SOPC Builder provided effective and less troublesome method of constructing and connecting the different hardware peripherals. The SOPC Builder generated Verilog modules for each of the components found in the RFID-Nios II Processor System. By properly instantiating the necessary components in the top module, the system was compiled successfully and the bitstream of it was downloaded to the FPGA board.

The software used in the study was constructed with the use of C language for matching the RFID tag index with respect to the assigned audio and textual file. The Nios II IDE was used for building, compiling, and debugging the C codes for the modules used in the whole system, such as the audio CODEC, LCD, and the SD card. Nios II IDE also made the group develop C codes easier because of its user friendly editor and helpful tutorials. The Hardware Abstraction Layer (HAL) device driver also reduced the difficulty in developing the C codes because it made the usual C functions possible and easier for the group to display text files on the LCD conveniently.

The ID-20 external peripheral proved to be an effective type of RFID reader and was easily applied using an RS232 serial interface. By using the reader to detect data stored in the RFID the tags, the corresponding audio files associated to an artifact in the museum was playedback.

For future works, a VGA display providing graphical information or a video playback can be developed to replace the 16x2 character LCD. The Audio CODEC using the standard WAV files can be replaced with an MP3 CODEC to reduce the file size of audio recordings thus, increasing the number of audio playbacks that can be stored.

5. REFERENCES

Tesoriero, R.; Gallud, J.A.; Lozano, M.; Penichet, V.M.R. (2008). *A Location-Aware System Using RFID and Mobile Devices for Art Museums.* Autonomic and Autonomous Systems, 2008. ICAS 2008. Fourth International Conference , vol., no., pp.76-81, 16-21 March 2008. Retrieved June 8, 2011, from http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4488325&isnumber=4488306

Altera Corp. (2009*). Quartus II Handbook 9.1, Volume 4: SOPC Builder System*, Retrieved June 20, 2012 from www.altera.com

Altera Corp. (2009*). Quartus II Handbook 9.1, Volume 5: Embedded Peripherals*, Retrieved June 20, 2012 from www.altera.com

Altera Corp. (2009*). Nios II Hardware Development Tutorial.* Retrieved October 4, 2012 from www.terasic.com

Altera Corp. (2009*). Nios II Software Developer's Handbook.* Retrieved October 4, 2012 from www.terasic.com

Altera Corp. (2010*). DE2 Development and Education Board User Manual.* Retrieved September 12, 2012 from www.altera.com